# HS-NM5500A

## Datasheet

**V1.2**

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## 1. Specification:

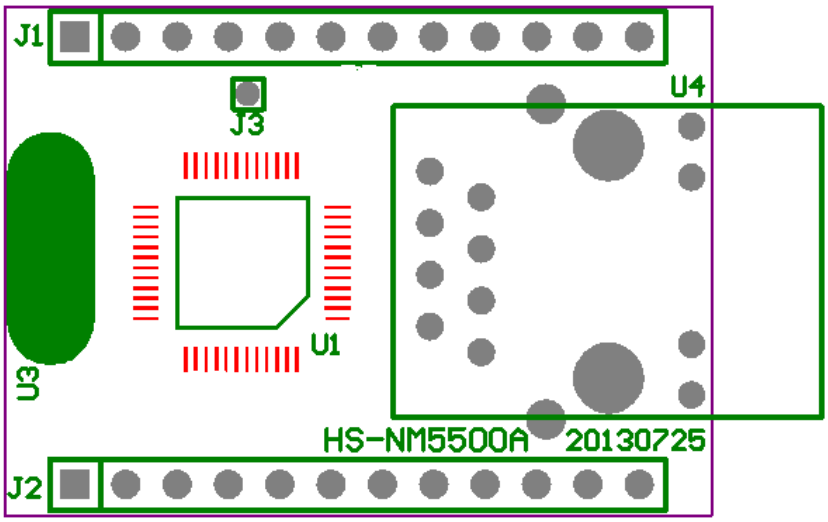
- Integrated W5500 and all necessary components within a compact PCB. The PCB is optimized and tested strictly;
- Keep W5500 all features;
- Provide high speed SPI to MCU interface;
- Enable Tx/Rx, Full/Half duplex, Link and Speed drive output;
- Operation voltage 3.3V, I/O pin has 5V tolerance;
- Embedded compact transformer inside RJ-45;
- Interface with two 2.54mm pitch 12 header pins;
- Operation temperature: -20~70℃

## 2. Photograph

HS-NM5500A has a RJ-45 Jack with transformer inside. The interface to MCU is two pitch 12 header pins.

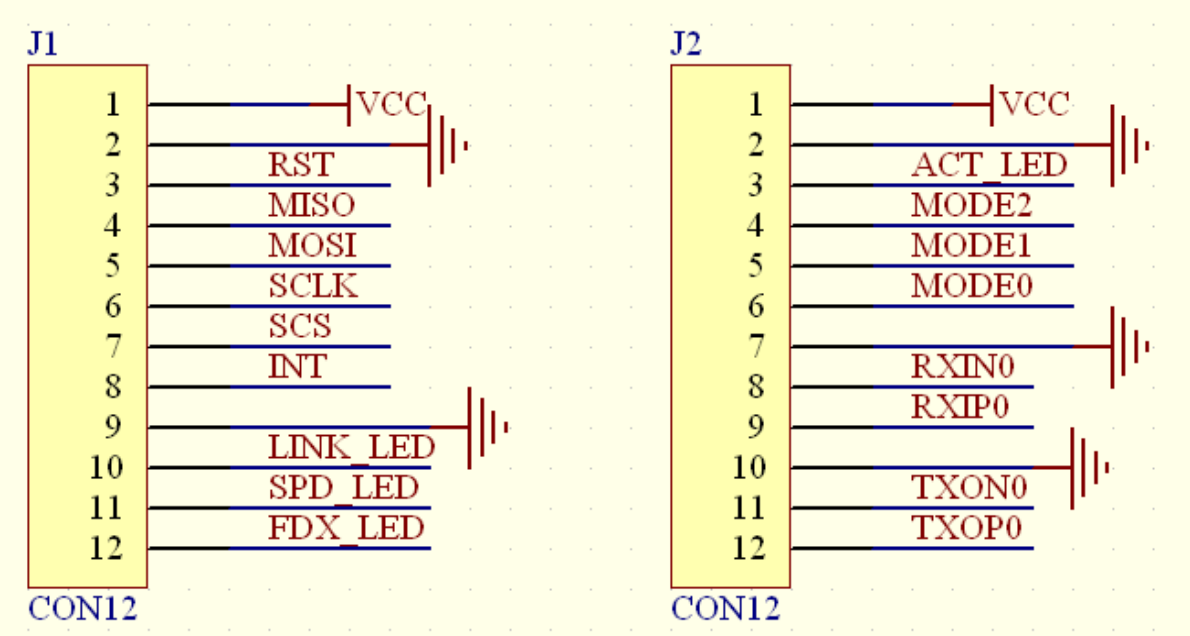

HS-NM5500A module

## 3. Layout




HS-NM5500A main components layout

J3 is a test point. In normal operation case, the voltage is 1.2V (Environment temperature at 25℃) at this point.



## Pin definition

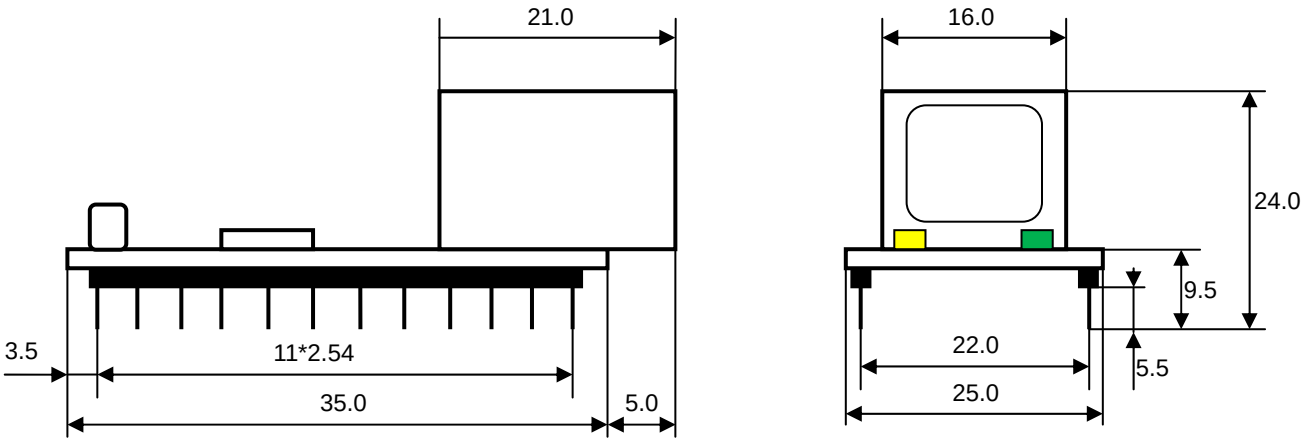
J1 Pin definition

| Pin | Name | Description |
|---|---|---|
| J1-1 | VCC | Power supply, at range 3.0~3.6V, typically 3.3V |
| J1-2 | GND | Power ground |
| J1-3 | /RST | RESET input, active low. The input RESET should be hold low at least 500us |
| J1-4 | MISO | SPI Bus, Master In Slave Out |
| J1-5 | MOSI | SPI Bus, Master Out Slave In |
| J1-6 | SCLK | SPI Bus, Clock signal |
| J1-7 | /SCS | SPI Bus, Chip select |
| J1-8 | /INT | Interrupt output, active low |
| J1-9 | GND | Power ground |
| J1-10 | LINK_LED | This shows the Link status.<br>Low: Link is established<br>High: Link is not established |
| J1-11 | SPD_LED | This shows the Speed status of the connected link.<br>Low: 100Mbps<br>High: 10Mbps |
| J1-12 | FDX_LED | This shows the Duplex status for the connected link.<br>Low: Full-duplex mode<br>High: Half-duplex mode |

J2 Pin definition

| Pin | Name | Description |
|---|---|---|
| J2-1 | VCC | Power supply, at range 3.0~3.6V, typically 3.3V |
| J2-2 | GND | Power ground |
| J2-3 | ACT_LED | It shows that there is Carrier Sense from the active Physical Medium Sub Layer during RX or TX activity<br>Low: Carrier Sense detected<br>High: No Carrier Sense |
| J2-4 | MODE2 | PHY Operation Select pins. Inner pull up.<br>These pins determine Ethernet PHY operation. For more information, please refer to W5500 datasheet. |
| J2-5 | MODE1 | |
| J2-6 | MODE0 | |
| J2-7 | GND | Power ground |
| J2-8 | TXOP | HS-NM5500A has no these signals output |
| J2-9 | TXON | |
| J2-10 | GND | Power ground |
| J2-11 | RXIP | HS-NM5500A has no these signals input |
| J2-12 | RXIN | |

## 4. Dimension (Unit: mm)



# 5. Parameters

## 5.1 DC parameters

(Test Condition: Ta = -40 to 85°C)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | Apply VDD, AVDD | 2.97 | 3.3 | 3.63 | V |
| $V_{IH}$ | High level input voltage | | 2.0 | | 5.5 | V |
| $V_{IL}$ | Low level input voltage | | - 0.3 | | 0.8 | V |
| $V_T$ | Threshold point | All inputs except XI | 1.30 | 1.41 | 1.53 | V |
| $V_{T+}$ | Schmitt trig Low to High Threshold point | All inputs except XI | 1.53 | 1.64 | 1.73 | V |
| $V_{T-}$ | Schmitt trig High to Low Threshold point | All inputs except XI | 0.95 | 1.02 | 1.09 | V |
| $T_J$ | Junction temperature | | 0 | 25 | 125 | °C |
| $I_L$ | Input Leakage Current | | | | ±1 | μA |
| $R_{PU}$ | Pull-up Resistor | SCSn, RSTn, PMODE[2:0] | 62 | 77 | 112 | Kohm |
| $R_{PD}$ | Pull-down Resistor | RSVD(Pin 23, Pin 38 ~ Pin 42) | 48 | 85 | 174 | Kohm |
| $V_{OL}$ | Low level output voltage | IOL = 8mA, All outputs except XO | | | 0.4 | V |
| $V_{OH}$ | High level output voltage | IOH = 8mA, All outputs except XO | 2.4 | | | V |
| $I_{OL}$ | Low level output Current | VOL = 0.4V, All outputs except XO | 8.6 | 13.9 | 18.9 | mA |
| $I_{OH}$ | High level output Current | VOH = 2.4V, All outputs except XO | 12.5 | 26.9 | 47.1 | mA |
| $I_{DD1}$ | Supply Current (Normal operation mode) | VDD=3.3V, AVDD=3.3V, Ta = 25°C | | 132 | | mA |
| $I_{DD2}$ | Supply Current (Power Down mode) | PHY Power Down mode, VDD=3.3V, AVDD=3.3V, Ta = 25°C | | 13 | | mA |

## 5.2 Power consumption

(Test Condition: VDD=3.3V, AVDD=3.3V, Ta = 25°C)

| Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 100M Link | - | 128 | - | mA |
| 10M Link | - | 75 | - | mA |
| Un-Link (Auto-negotiation mode) | - | 65 | - | mA |
| 100M Transmitting | - | 132 | - | mA |
| 10M Transmitting | - | 79 | - | mA |
| Power Down mode | - | 13 | - | mA |

## 5.3 Reset timing

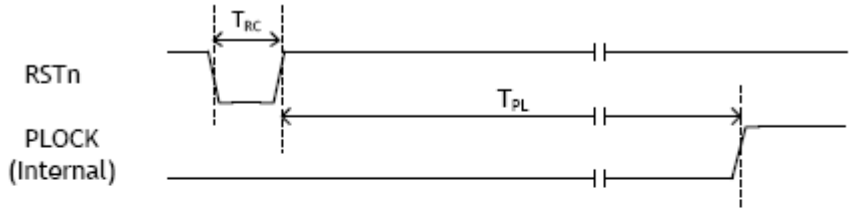



Figure 22. Reset Timing

| Symbol | Description | Min | Max |
|---|---|---|---|
| $T_{RC}$ | Reset Cycle Time | 500 us | - |
| $T_{PL}$ | RSTn to internal PLOCK (PLL Lock) | - | 1 ms |

**Please refer to W5500 datasheet to get more information.**